Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor wafer comprising:

a first conduction type low concentration impurity layer formed beneath a principal face of a wafer to a predetermined depth;

a first conduction type high concentration impurity layer directly underlying said low concentration impurity layer; and

a first conduction type high concentration impurity diffusion region formed along at least a portion of the dicing lines that delimit a plurality of chips on said wafer, said diffusion region extending from the principal face of the wafer to said high concentration impurity layer, wherein said diffusion region has a width larger than that of the cutting allowance for the dicing along the dicing lines.

2. (Original) A semiconductor wafer according to claim 1, wherein said high concentration impurity diffusion region has a lattice-shaped pattern.

3. (Original) A semiconductor wafer according to claim 1, wherein said high concentration impurity layer has a resistance value not higher than 0.05 Ω·cm.

4. (Currently amended) A semiconductor device comprising:

a first conduction type low concentration impurity layer;

a first conduction type high concentration impurity layer directly underlying said low concentration impurity layer; and

a first conduction type high concentration impurity diffusion region that extends from the upper surface of said low concentration impurity layer to said high concentration impurity layer, said diffusion region being positioned at the outer edge of an element region having a semiconductor element formed therein,

wherein said diffusion region comprises a portion or the entirety of dicing regions on a wafer containing said device.

5. (Original) A semiconductor device according to claim 4, wherein said high concentration impurity layer has a resistance value not higher than 0.05 Ω·cm.

6. (Currently amended) A semiconductor device ~~according to claim 4,~~ comprising:

a first conduction type low concentration impurity layer;

a first conduction type high concentration impurity layer underlying said low concentration impurity layer; and

a first conduction type high concentration impurity diffusion region that extends from the upper surface of said low concentration impurity layer to said high concentration impurity layer, said diffusion region being positioned at the outer edge of an element region having a semiconductor element formed therein,

wherein said diffusion region comprises a portion or the entirety of dicing regions on a wafer containing said device, and

wherein said element region comprises a power semiconductor element and a control circuit for controlling said power semiconductor element.

7. (Original) A semiconductor device according to claim 4, wherein said high concentration impurity diffusion region is electrically connected with at least one electrode formed on the upper surface of said low concentration impurity layer.

8. (Original) A semiconductor device according to claim 4, wherein said high concentration impurity diffusion region electrically connects said high concentration impurity layer with at least on electrode positioned above said low concentration impurity layer.

9. (Currently amended) A semiconductor device ~~according to claim 5,~~ comprising:

a first conduction type low concentration impurity layer;

a first conduction type high concentration impurity layer underlying said low concentration impurity layer, said high concentration impurity layer having a resistance value not higher than 0.05 Ω·cm; and

a first conduction type high concentration impurity diffusion region that extends from the upper surface of said low concentration impurity layer to said high concentration impurity layer, said diffusion region being positioned at the outer edge of an element region having a semiconductor element formed therein,

wherein said diffusion region comprises a portion or the entirety of dicing regions on a wafer containing said device, and

wherein a plurality of high concentration impurity diffusion regions connect said high concentration impurity layer to a plurality of electrodes positioned above said low concentration impurity layer.

10. (Withdrawn-Currently amended) A process for manufacturing a semiconductor device, comprising:

forming a first conduction type high concentration impurity diffusion region in a semiconductor wafer, said wafer comprising a first conduction type low concentration impurity layer directly overlying a first conduction type high concentration impurity layer, wherein said diffusion region extends from an upper surface of said high concentration region to said low concentration layer and is formed along a portion or the entirety of dicing lines to be used for cutting said wafer into a plurality of chips, and wherein said diffusion region has a width larger than that of the cutting allowance for the dicing tool;

forming an element in said semiconductor wafer; and

cutting said semiconductor wafer in which an element is formed into individual chips by dicing.

11. (Withdrawn) A semiconductor device manufacturing process according to claim 10, wherein said high concentration impurity diffusion region is formed by covering said wafer with a mask and exposing it only along a portion or the entirety of the dicing lines to a high-temperature gas containing an impurity.

12. (Withdrawn) A semiconductor device manufacturing process according to claim 10, wherein said high concentration impurity diffusion region is formed by covering only a portion or the

entirety of the dicing lines with a material containing an impurity, and by leaving it at a high temperature.

13. (Withdrawn) A semiconductor device manufacturing process according to claim 10, wherein said high concentration impurity diffusion region is formed by ion implantation.